REMARKS/ARGUMENTS

The Applicants originally submitted Claims 1-16 in the application. In previous responses, the Applicants added Claims 17-19 and amended Claims 4, 7-9 and 12-16. The Examiner has indicated that Claims 7-13 are allowable and that Claims 3-5 and 15 would be allowable if rewritten in independent form. In response, the Applicants have amended Claims 1, 14 and 18 and have added Claim 20. Additionally, the Applicants have canceled Claim 17. Accordingly, Claims 1-16 and 18-20 are currently pending in the application.

I. Rejection of Claims 17-18 under 35 U.S.C. §112

The Examiner has rejected Claims 17-18 under 35 U.S.C. §112, second paragraph, for being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicants regard as the invention. Regarding Claim 17, the Examiner questions how the admittance stage can be "configured" to produce a "data output." For Claim 18, the Examiner questions how the transistors can lack a common coupling point. (*See* Examiner's Action, page 2.)

In response, the Applicants have canceled Claim 17 and amended Claim 18. Accordingly, the Applicants respectfully request that the Examiner withdraw the §112, second paragraph, rejection and allow issuance of amended Claim 18.

II. Rejection of Claims 1-2, 6, 14, 16 and 18-19 under 35 U.S.C. §102

The Examiner has rejected Claims 1-2, 6, 14, 16 and 18-19 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,276,488 to Benedict, *et al.* (Benedict). The Applicants respectfully disagree.

Benedict is directed to computer logic circuits and, more particularly, to an array of multi-master single-slave flip-flop circuits that can be disposed on a single large-scale IC chip. (*See* column 1, lines 5-8.) Benedict teaches a simplified master-slave flip-flop circuit with the master and slave circuits having a two-level cascode circuit with lower current switch transistors 31 and 33 and an input upper current switch coupled to a circuit of transistors 40-43. (*See* column 4, lines 54-60 and Figure 2.) The Examiner asserts that the circuit of transistors 40-43 is an active load as recited in independent Claim 1. (*See* Examiner's Action, page 3.)

Benedict does not teach, however, a latch including an active load connected to receive as input the current output of a trans-admittance circuit and produce a voltage output that is received by the trans-admittance circuit as recited in Claim 1. On the contrary, the output (QM1) of the circuit of transistors 40-43 is sent to the slave circuit, not the lower current switch transistors 31-33. (*See* Figure 2.)

Benedict, therefore, does not disclose each and every element of Claim 1 and Claims dependent thereon. Accordingly, Benedict does not anticipate Claims 1-2 and 6 and the Applicants respectfully request the Examiner to withdraw the §102 rejection and allow issuance thereof.

Additionally, Benedict does not teach a latch pair including a first combined trans-admittance and trans-impedance stage and an independent second combined trans-admittance and trans-impedance stage as recited in independent Claim 14. On the contrary, Benedict teaches a master latch circuit 20-1 and a slave latch circuit 21 that is dependent on the master latch circuit 20-1. (*See* column 4, lines 54-56 and Figure 2.) Benedict, therefore, does not disclose each and every element of Claim 14 and Claims dependent thereon. Accordingly, Benedict does not anticipate Claims 14,

16 and 18-19 and the Applicants respectfully request the Examiner to withdraw the §102 rejection and allow issuance thereof.

III. Conclusion

In view of the foregoing amendment and remarks, the Applicants now see all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1-16 and 18-20.

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

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